

**James A. Marek**  
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**Synopsis**

Experienced digital designer at the ASIC, FPGA/PLD, Board, and System level and have developed software for all aspects of design. I have extensive experience in design and simulation in various environments with numerous tools. I have a very short learning curve.

**Work History**

Jan 1990 - Present  
Rockwell Collins Inc.  
Sr. Design Engineer

Member of a small team who developed proprietary stack based microprocessors for avionics applications and developed the worlds first direct execution Java microprocessor (JEM). Developed microprocessor based boards for various functions including 10/100 base T dual redundant ethernet, graphics with XGA LCD output controller, Multiple channel redundant fiber channel based fiberoptic display interface. Member of small team who developed graphics rendering system ASICs for all Rockwell Collins displays. Developed X-windows based tool in C for simulating temporal modulation scheme for driving passive matrix LCD panels. Developed test equipment pods for microprocessor debugging tool suite. Developed production tests and release documentation for several microprocessor ASICs. Performed fault testing and analysis using Zycad for several ASICs.

Jan 1987 - Dec 1989  
Rockwell Collins Inc.  
Engineering Co-op

Performed schematic capture, digital design, board level debug, FORTRAN and Pascal programming for GPS Test Equipment Group, and Advanced Technology Microprocessor Group.

**Relevant Skills & Technologies**

Behavioral and structural VHDL and Verilog for synthesis and modeling. FPGA, EPLD, PAL design, simulation, and debug  
Standard cell and full custom ASIC design.  
Microprocessor architecture and system design, testing, and debug.  
JTAG test interfaces for ASICs  
BIST for ASICs memory, logic, and datapath  
Microcode for microcoded microprocessors  
Graphics rendering subsystems and LCD output controllers  
Fiber-Channel fiber-optics interfaces  
10/100 base T Ethernet  
LVDS interfaces  
PCI and ISA bus memory and IO mapped.  
Project management of teams less than 10 engineers and technicians  
Department and section level R&D planning  
I have had training in OOA and OOD

**Tools**

Synopsys Design Compiler, Mentor Modelsim, Avant!, Altera Maxplus tools, Synplicity Synplify, Chronology Timing Designer, Compass tools (schematic, VHDL, datapath, ram/rom compilers, sc layout, full custom layout), Viewlogic tools, Chrysalis Design Verifier, Racal Redac tools, Zycad Fault tools, Interleaf, MS Office tools.

<b>Environments</b>	UNIX, Windows XP, NT, 95, 3.1, Linux, Mac OS, X-windows
<b>Languages</b>	C, Perl, VHDL, Verilog, JAVA, UNIX shell scripting, HTML, Ada, Pascal, FORTRAN
<b>Education</b>	1994 MS Computer Engineering, Iowa State University, Ames IA GPA:3.96/4.00 1989 BS Computer Engineering, Iowa State University, Ames IA GPA:3.69/4.00
<b>Special Mention</b>	Passport is current
<b>References</b>	Available upon request